Thermal Scanning Probe Lithography and its Applications

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Thermal scanning probe lithography (t-SPL) has recently entered the lithography market as first true alternative to electron beam lithography (EBL). By now, the first dedicated t-SPL systems, *NanoFrazors*®, have been installed at research facilities in Europe, America, Asia and Australia by the company SwissLitho, a spinoff company from ETH Zurich.

Core of the technology - which has its origins at IBM Research and their Millipede project - is a heatable probe tip which is used for patterning and simultaneous inspection of complex nanostructures (Figure 1a). The heated tip creates very high-resolution (< 10 nm half-pitch) nanostructures by locally evaporating resist materials. The patterning depth can be controlled with 1 nm accuracy, enabling patterning of extremely accurate 3D topographies (Figure 1b) in a single step.

The patterning speed of t-SPL is comparable to that of high-resolution Gaussian shaped EBL, and a scan speed of 20 mm/s with a pixel rate of 500 kHz has been demonstrated. The written nanostructures are inspected by the cold tip in parallel with the patterning process, enabling new methods for stitching and overlay with sub-5 nm accuracy without the use of artificial marker structures.

Pattern transfer methods based on reactive ion etching, lift-off, electroplating, directed self-assembly and more have been demonstrated in combination with t-SPL. Various application examples demonstrating the unique capabilities of the *NanoFrazor*® will be shown, for example 3D optical devices such as phase plates, gratings and computer generated holograms. Furthermore, devices with graphene or MoS_2 flakes, carbon nanotubes and nanowires (Figure 1c) will be shown. Such devices benefit from the accurate overlay capability and the fact that no charged particle beam that might degrade the sensitive materials is used during the lithography.

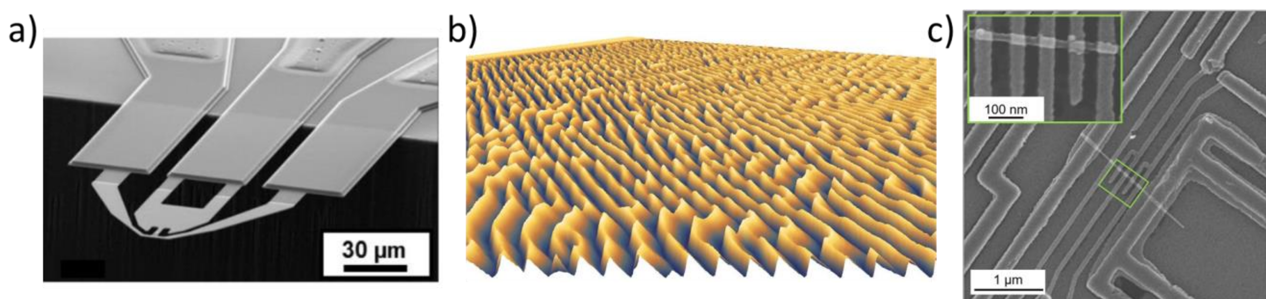

Figure 1 (a) SEM image of the Si cantilever used for t-SPL including an integrated heater, topography sensor, electrostatic actuation and an ultra-sharp tip (< 5 nm radius). (b) AFM image of a 3D hologram patterned by t-SPL. (c) SEM image of an InAs nanowire transistor. 50 nm wide interdigitated top gates were fabricated by lift-off with very accurate overlay and without damage to the nanowire or the gate oxide.